

20. [New] The system according to claim 1, further comprising:
a channel-node circuit chip, the chip having an on-chip data buffer; and
an off-chip memory operatively coupled to supply data to the channel-node circuit chip,
wherein the communications channel is an fibre channel arbitrated loop, and the loop is held
open if at least one-half a frame of data is contained in on-chip data-frame buffer, and at least one
frame of data are contained in off-chip memory.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on September 26, 2000, and the references cited therewith.

Claims 1, 2 and 8-10 are amended, and claims 18-20 are added; as a result, claims 1-20 are now pending in this application.

§103 Rejection of the Claims

Claims 1, 7-8, and 16-17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's submission of prior art [AAPA], and Pritty et al. (U.S. Patent No. 4,819,229).

Applicant respectfully traverses the rejection. Pritty describes (according to its abstract):

"A LAN priority control system is described which uses an interrupt priority control structure which suspends transmission of a packet from a lower priority node and allows a higher priority interrupting node, which desires to transmit a higher priority message, to obtain rapid access to the transmission medium and to transmit the message. The message is interrupted using a within packet interrupt which is taken to include any command which results in the transmission of a packet onto a common-medium being halted before the complete packet has been transmitted."

Pritty further describes

"node 1 detects the on state of the interrupt channel and then decides [whether] to interrupt the data transfer of the packet. This depends on the amount of untransmitted data. For example, an algorithm [sic] is present in the node which recognises [sic] the percentage of data still to be transmitted and if the amount of data is less than for example 10% of the total data or a fixed number of bytes e.g. 100 bytes the interrupt request would be ignored and the message completed."

However, if more than 10% data is remaining, then the interrupt is accepted (column 7 lines 21-32). Thus, although a high-priority interrupt (passed as a token on the baseband LAN) would normally stop transmission of the packet, if the transmission is close enough to finishing (at most 10% or 100 bytes remaining), it will be allowed to finish by temporarily ignoring the

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interrupt request.

In contrast, claims 1 and 8 and their dependent claims of the present invention are drawn to apparatus that maintains control of the communications channel as long as **at least** a second predetermined amount of data is available within control of the channel node, even though some data may not be available for transfer (see claim 1 as amended):

“an arbitration-and-control apparatus to reduce arbitrated-loop overhead, wherein the arbitration-and-control apparatus arbitrates for control of a loop of the communications channel and, after control is achieved, maintains control of the communications channel as long as at least a first predetermined amount of data is available within control of the channel node, wherein the first predetermined amount of data within control of the channel node includes at least some data not available for transfer.”

The present invention provides a mechanism for controller architecture designs which allows the communications channel (or loop) to be held open by a port if data will shortly be available to the port. This can reduce the number of times a node interface of loop port must arbitrate during an outgoing data transfer, and may thus allow transfers to complete sooner by allowing the loop to be held open in anticipation of sufficient further data becoming available to a port in order to justify that port's retaining control of the loop. (see page 45 of the specification). Accordingly, claim 1 and its dependent claims and claim 8 and its dependent claim appear to be in condition for allowance, and such action is respectfully requested.

Regarding claim 10, a method is recited. This method (as amended) includes

“maintaining control of the loop of the communications channel as long as a first predetermined minimum amount of data is available within control of the channel node, wherein the first predetermined amount of data within control of the channel node includes at least some data not currently available for transfer, whereby arbitrated-loop overhead is reduced.”

This too distinguishes from the cited prior art and the combination proposed by the Examiner. Accordingly, claim 10 and its dependent claims appear to be in condition for allowance, and such action is respectfully requested.

Regarding claims 16-17, Applicant respectfully traverses the rejection. Claim 16 recites “arbitration-and-control means for reducing arbitrated-loop overhead.” Accordingly, this claim must be Examined under 35 U.S.C. §112¶6. ¶6 allows inventors to define or claim features of their inventions as a “means” or “step” for performing a function without literally reciting

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structure, material, or acts in the claim itself for performing the function. However, ¶6 also limits the interpretation of these claimed features to the corresponding structure, material, or acts described in the present specification and their structural equivalents. For example, one may claim an element of an invention as “a means for fastening two boards.” Literally, this language encompasses screws, nails, glue, clamps, indeed anything that could serve the fastening function. Yet, ¶6 requires the Examiner and courts to look to the specification to determine a claim's legal scope. The Court of Appeals for the Federal Circuit in the case *In re Donaldson Inc.*, 29 USPQ2d 1845 (CAFC Feb. 14, 1994) said:

“ The plain and unambiguous meaning of paragraph six is that one construing means-plus-function language in a claim must look to the specification and interpret that language in light of the corresponding structure, material, or acts described therein, and equivalents thereof, to the extent that the specification provides such disclosure. **Paragraph six does not state or even suggest that the PTO is exempt from this mandate, and there is no legislative history indicating that Congress intended that the PTO should be.**”

Ibid, 29 USPQ2d at 1848 (emphasis added). Thus, the PTO is required by statute to look to the Applicant's specification and to construe the “means” language recited in claims 16 and 17 as limited to the corresponding structure disclosed in the specification and equivalents thereof. *See* 29 USPQ2d at 1850. The Examiner has not met his burden of showing equivalent structure, material, or acts in the prior art that would anticipate claims 16 and 17 as interpreted under 35 U.S.C. §112¶6. Accordingly, claims 16 and 17 appear in condition for allowance, and withdrawal of the rejection is respectfully requested.

Claims 2-6 and 9 and 10-15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's submission of prior art [AAPA], Pritty et al. (U.S. Patent No. 4,819,229), and Birns et al. (U.S. Patent No. 6,012,128). Applicant respectfully traverses the rejection. Birns describes (see column 2 line 21-45):

“ The present invention is directed to a 16-bit microcontroller system that includes an address space of preferably 16 megabytes (Mb) and includes a page zero mode where only a first or zeroth page of 64 kilobytes (Kb) is addressed. ...

The architecture of the microcontroller system 10 of the present invention is illustrated in FIG. 1. This system 10 includes a single chip microcontroller 12 that performs 16-bit arithmetic operations and includes internal instruction and data storage preferably configured with from 8 Kb to 64 Kb. The microcontroller 12 supports external devices 14 and 16 and, through 24 bit external address capability, supports sixteen megabytes of external instruction storage 18 and sixteen megabytes of external data storage 20. ”

Thus Birns merely provides a microcontroller chip having on-chip RAM and allowing off-chip

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RAM-- it does not provide on chip and off chip buffers both holding data to be transferred on a channel, nor is an amount of data measured and compared to a predetermined value. Further, even if combined with AAPA and Pritty, a single predetermined amount that accounts for both on-chip and off-chip data is not done, and separate predetermined amounts of on-chip and off-chip data are not compared.

In contrast, claim 1 and claim 9 (as amended) of the present invention recite:

“a channel-node circuit chip, the chip having an on-chip data buffer, wherein the first predetermined amount of data includes a predetermined amount of on-chip data within the on-chip data buffer currently available for transfer to the communications channel; and

an off-chip memory, wherein the first predetermined amount of data further includes a predetermined amount of off-chip data, which is to be transferred to the communications channel but is currently not available for transfer, within the off-chip memory that is distinct from the predetermined amount of on-chip data.”

Accordingly, both claim 2 and its dependent claims 3-6 and claim 9 appear to be in condition for allowance, and withdrawal of the rejection is respectfully requested.

Regarding claim 11, a method is recited. This method includes

- “ (b)(I) determining an on-chip amount of data available in a channel-node circuit chip;
 (b)(ii) determining an off-chip amount of data available in an off-chip memory; and
 (b)(iii) comparing the on-chip amount of data available to a predetermined minimum-required amount of on-chip data;
 (b)(iv) comparing the off-chip amount of data available to a predetermined minimum-required amount of off-chip data; and
 (b)(v) maintaining control of the loop based on these comparisons.”

Pritty does not compare to a minimum-required amount of data, but rather to a maximum allowed amount (i.e., interrupts are allowed if more than this amount remains). Pritty further only looks at one source of data for comparison, not two. Since Pritty provides only one memory and one comparison, the Examiner's contentions that it would have been obvious to have two predetermined amounts, or to set the off-chip amount to be different than the on-chip amount are totally unfounded. The Examiner has failed to provide a *prima facie* case of obviousness. Accordingly, claim 11 and its dependent claims 12-15 appear to be in condition for allowance, and withdrawal of the rejection is respectfully requested.

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AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

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Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6949 to facilitate prosecution of this application. If necessary, please consider this a petition for extension of time in the necessary number of months, and please charge any required additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JUDY LYNN WESTBY ET AL.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 23 day of March 23, 2001.

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